

FAIRCHILD MEMORIES

RANDOM ACCESS MEMORIES

BIPOLAR RAMs

Item	Organization	DEVICE NO.	Description <sup>(1)</sup>	Address Access Time ns (Typ)	Chip Select Access Time ns (Typ)	Read/Write Cycle Time		Power Dissipation mW (Typ)	Logic/Connection Diagram	Package(s)
						Comm 0°C to +70°C ns (Max)	-55°C to +125°C ns (Max)			
TTL										
1	16x4	54LS/74LS89 <sup>(4)</sup>	OC	—	—	—	—	—	M1	4L,7B,9B
2	16x4	54LS/74LS189 <sup>(4)</sup>	3S	—	—	—	—	—	M1	4L,7B,9B
3	16x4	54LS/74LS289 <sup>(4)</sup>	OC	—	—	—	—	—	M1	7B,9B
4	16x4	7489	OC	30	30	60/55	60/55	—	M1	4L,7B,9B
5	16x4	9410	3S	35	25	50 <sup>(2)</sup>	—	375	M50	7D,9M
6	256x1	93410	OC	45	25	60/45	70/55	450	M2	4B,6F,9B
7	256x1	93410A	OC	35	20	45	—	450	M2	6D,9B
8	256x1	93411	OC	45	25	55/45	65/55	475	M3	4B,6D,9B
9	256x1	93411A	OC	40	25	45	—	475	M3	6D,9B
10	256x1	93L420	3S	40	20	45	55	250	M3	4B,6D,9B
11	256x1	93L421	3S	45	30	90/75	100/90	275	M3	4B,6D,9B
12	256x1	93421	3S	35	20	50/35	60/45	475	M3	4B,6D,9B
13	256x1	93421A	3S	30	20	40/35	—	475	M3	6D,9B
14	64x9	93419	OC	35	15	45	60	725	M4	7Y
15	256x4	93412	OC	30	20	45	60/55	475	M5	4K,4R,8T
16	256x4	93L412	OC	45	20	60	75/70	250	M5	4K,4R,8T
17	256x4	93422	3S	30	20	45	60/55	475	M5	4K,4R,8T
18	256x4	93L422	3S	45	20	60	75/70	250	M5	4K,4R,8T
19	1024x1	93415	OC	30	15	45	60	475	M6	4B,6D,9B
20	1024x1	93L415	OC	35	20	60	70	200	M6	4B,6D,9B
21	1024x1	93415A	OC	25	15	30	—	475	M6	6D,9B

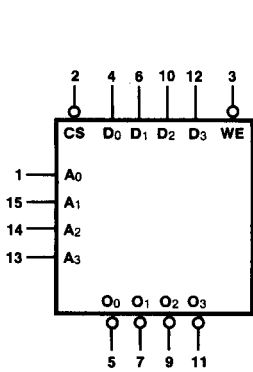
1. OC = open collector, 3S = 3-state
2. Measured @ T<sub>A</sub> = 25°C
3. Typical Data In to Match Out
4. To be announced

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# FAIRCHILD LOGIC/CONNECTION DIAGRAMS

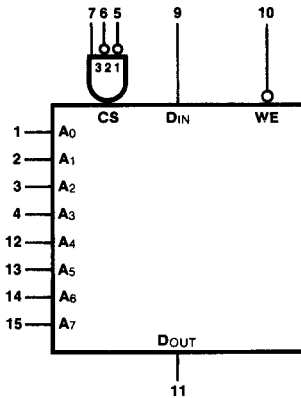
## MEMORY

**M1**  
54LS/74LS89, 54LS/74LS189,  
54LS/74LS289, 7489



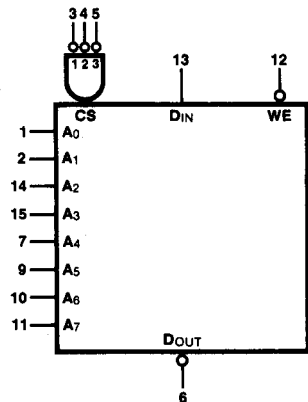
V<sub>CC</sub> = Pin 16  
GND = Pin 8

**M2**  
93410, 93410A



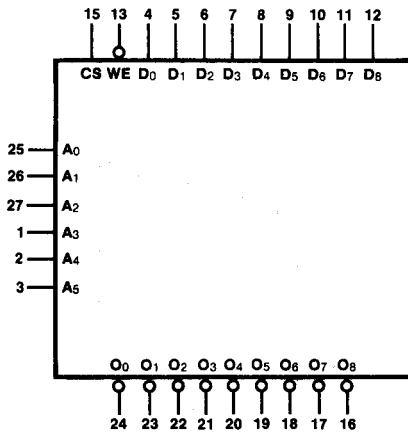
V<sub>CC</sub> = Pin 16  
GND = Pin 8

**M3**  
93411, 93411A, 93L420,  
93L421, 93421, 93421A



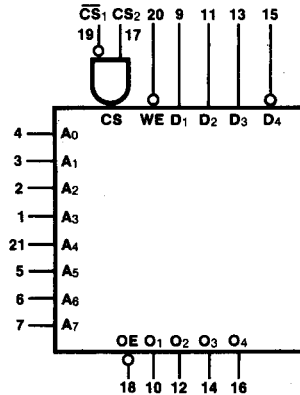
V<sub>CC</sub> = Pin 16  
GND = Pin 8

**M4**  
93419



V<sub>CC</sub> = Pin 28  
GND = Pin 14

**M5**  
93412, 93L412  
93422, 93L422



V<sub>CC</sub> = Pin 22  
GND = Pin 8